PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of	Docket No: Q78432
Hien Boon TAN, et al.	
Appln. No.: 10/721,382	Group Art Unit: 2894
Confirmation No.: 6007	Examiner: David E. Graybill
Filed: November 26, 2003	

For: HIGH PERFORMANCE CHIP SCALE LEADFRAME PACKAGE METHOD OF MANUFACTURING

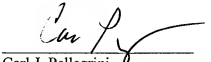
SUBMISSION OF APPEAL BRIEF

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith please find an Appeal Brief. The USPTO is directed and authorized to charge the statutory fee of $540.00 and all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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Date: March 24, 2009

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APPEAL BRIEF UNDER 37 C.F.R. § 41.37

MAIL STOP APPEAL BRIEF - PATENTS
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Sir:

In accordance with the provisions of 37 C.F.R. § 41.37, Appellant submits the following:

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I. REAL PARTY IN INTEREST

The real party in interest in this appeal is UNITED TEST AND ASSEMBLY TEST CENTER LTD.. Assignment of the application was submitted to the U.S. Patent and Trademark Office on November 26, 2003, and recorded on the same date at Reel 014744, Frame 0665.

II. RELATED APPEALS AND INTERFERENCES

To the best of the knowledge and belief of Appellant, Appellant's legal representatives, and the Assignee, there are no other appeals or interferences that will directly affect or be affected by the Board's decision in the present Appeal.

III. STATUS OF CLAIMS

Claims 25 and 26 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,825,062 (Yee) and U.S. Patent No. 6,710,430 (Minamio).

Claims 1-24 and 27 have been previously cancelled.

The rejections of claims 25 and 26 are being appealed.

IV. STATUS OF AMENDMENTS

An after-final amendment was filed on January 9, 2009. The amendment canceled claim 27 to put the application in better condition for appeal. The Advisory Action dated January 15, 2009 does not indicate whether the amendment entered. However, it states that the rejected claims are only claims 25 and 26.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The claimed invention relates to method assembling an improved high density chip scale leadframe package. [0003] See for example figures 2A and 8A, B, C and D.

More specifically, a method of assembling an IC package includes providing a leadframe 820 having a first face and a second face opposite to the first face. The leadframe includes an outer frame portion 825, a die pad portion 823, a plurality of tie bars 824 connecting the die pad portion 823 to the outer frame portion 825, and a plurality of protuberances 826 extending substantially radially inward from the outer frame portion 825. The die pad portion 823 is substantially centrally disposed within the outer frame portion 825. Each of the plurality of protuberances comprises an inner lead portion 827, an outer lead portion 828, and a post portion 829 connecting the inner lead portion 827 to the outer lead portion 828. the method further comprises providing an IC chip 805 having a first face 805a and a second face 805b opposite to the first face, a first plurality of wires 811 each having a first end 811a and a second end 811b, and a second plurality of wires 812 each having a first end 812a and a second end 812b. [0057]

The method further includes disposing an adhesive layer 804 on the first face of the leadframe. As illustrated in Figure 8B, the adhesive layer 804 covers the die pad portion 823, and part of the inner lead portion 827 of each of the plurality of protuberances 826. Part of each inner lead portion 827 of each of the plurality of protuberances 826 remains free from adhesive 804. According to one aspect of the present embodiment, and as illustrated in Figure 8D, the adhesive layer 804 can be disposed only on an outer edge of the die pad portion 823, thereby leaving a central window of the die pad portion 823 free from adhesive. [0058]

Next, to the claimed invention includes mechanically or chemically severing the inner lead portions 827 from the outer lead portions 828 by cutting the post portions 829. The method also includes mounting the IC chip 205 on the leadframe 820 whereby the second face 205b of the IC chip 205 is connected to the first face of the die pad portion 823 and to the first faces of each of the plurality of inner lead portions 827 through the adhesive layer 804. As described with respect to the sixth exemplary embodiment of the present invention, this step provides stability to the overall IC package and maintains the inner lead portions 824 in their proper positions. [0059]

The method further includes electrically conductively joining the first end 211a of each of the first plurality of wires 211 to the first face of one of the plurality of inner lead portions 827 and electrically conductively joining the second end 211b of each of the first plurality of wires 211 to the first face 205a of the IC chip 205. The method further comprises electrically conductively joining the first end 212a of each of the second plurality of wires 212 to the first face of one of the plurality of outer lead portions 828 and electrically conductively joining the second end 212b of each of the second plurality of wires 212 to the first face 205a of the IC chip 205. [0060]

The subject matter of the independent claim, with reference to the specification and figures, is identified below.

25. A method of assembling an integrated circuit package [figure 2A], comprising:

a) providing:

a leadframe [item 820, figures 8A-D] having a first face and a second face opposite to said first face, wherein said leadframe comprises:

an outer frame portion [item 825, figure 8A],

a die pad portion substantially centrally disposed within said outer frame portion [item 823, figures 8A, D],

a plurality of tie bars [item 824, figure 8A] connecting said die pad portion to said outer frame portion, and

a plurality of protuberances [item 826, figure 8A] extending substantially radially inward from said outer frame portion [item 825, figure 8A], each of said plurality of protuberances comprising an inner lead portion [item 827, figures 8A-C], an outer lead portion [item 828, figures 8A-C], and a post portion [item 829, figures 8A, B] connecting said inner lead portion from said outer lead portion,

an integrated circuit chip [item 205, figure 2A] having a first face [item 205A, figure 2A] and a second face [item 205b, figures 2A] opposite to said first face,

a first plurality of wires [item 211, figure 2A] each having a first end [item 211a, figure 2A] and a second end [item 211b, figure 2A], and

a second plurality of wires [item 212, figure 2A] each having a first end [item 212a, figure 2A] and a second end [item 212b, figure 2A];

b) disposing an adhesive layer [item 804, figures 8B-D] on said first face of said leadframe, whereby said adhesive layer covers said die pad portion, and part of said inner lead

portion of each of said plurality of protuberances, wherein part of each of said inner lead portions remains free of adhesive [figures 8B-D] [0058];

c) severing said outer lead portion from said inner lead portion by cutting said post portion [0059];

d) mounting said integrated circuit chip on said leadframe, whereby said second face of said integrated circuit chip is connected to a first face of said die pad portion through said adhesive layer, and whereby said second face of said integrated circuit is further connected to said inner lead portions through said adhesive layer [0059];

e) electrically conductively joining said first end of said first plurality of wires to a first face of one of said plurality of inner lead portions [0060];

f) electrically conductively joining said second end of each of said first plurality of wires to said first face of said integrated circuit chip [0060];

g) electrically conductively joining said first end of each of said second plurality of wires to a first face of one of said outer lead portions [0060], and

h) electrically conductively joining said second end of said second plurality of wires to said first face of said integrated circuit chip [0060].

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellant requests that the following rejections be reviewed:

Claims 25 and 26 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,825,062 (Yee) and U.S. Patent No. 6,710,430 (Minamio).

No other grounds of rejection or objection currently are pending.

This appeal is directed to claims 25 and 26.

VII. ARGUMENT

The rejection of claims 25 and 26 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,825,062 (Yee) and U.S. Patent No. 6,710,430 (Minamio).

Appellant respectfully requests the members of the Board to reverse the aforementioned rejection of claims 25 and 26 under 35 U.S.C. §103(a) as allegedly being unpatentable over Yee in view of Minamio because one skilled in the art would not have combined the teachings of Yee and Minamio to arrive at the claimed invention.

Yee discloses methods of fabricating lead frame packages having lead separation preventing means (see Col. 12, lines 17-18). Although not shown in Fig. 7A referred to in Col. 12, lines 17-18, one of skill in the art would understood from the remaining disclosures in Yee that the lead separation preventing means includes a lead lock, referred to as element 14 in the figures, that is formed on the inner ends of the leads to maintain the leads in position when impacted during singulation. Yee also discloses the use of an adhesive on the die pad and the inner leads to eliminate a short circuit from occurring should the leads come into contact with the lower surface of the semiconductor chip (see Col 12, lines 41-45).

Yee, however, only discloses single row leads surrounding the die paddle and therefore does **not** disclose the feature of the post portions and severing of the post portions to create dual or more rows of leads without affecting the overall stability of the IC structure. Moreover, the teachings of Yee do not suggest that stability of the package is by reason of the die being mounted onto the die pad and portions of the inner leads as defined in claim 25 of the present application.

The method of the claimed invention as defined by claim 25 fabricates a multi-row lead frame package. By having post portions which connect the inner leads to the outer leads, and severing the post portions to create dual or (more) rows of leads, mechanical impact on the overall structure is reduced during the severing, thereby maintaining the leads in position and possible deformation of the overall structure. Also, the integrated circuit chip being mounted onto the lead frame in a manner such that second face of the chip is connected to the first face of the die pad and a portion of the inner leads, improves stability of the overall IC structure. The combination of both features advantageously provides the desired stability to the overall structure of the IC package and maintains proper position of the leads.

Minamio discloses lead frame packages with muti-rows of leads and that the first lead and third lead are physically and electrically separated by punching through the connecting portion Rcnct (see Col. 8, lines 7-20; Col. 11, lines 28-29). Minamio also teaches that the leads are separated to prevent crosstalk from occurring (see Col. 11, lines 28-39).

Minamio, however, does not teach or suggest that the connecting portion (post portion) between the first and third leads (i.e., inner and outer leads) is designed such that severing thereof would maintain stability to the structure and maintain the position of the leads. The severing of the connecting portions in Minamio merely functions to separate the first and third leads so that cross talk can be prevented.

Minamio also does not disclose the integrated circuit chip being mounted onto the leadframe in a manner such that the second face of the chip is connected to the first face of the die pad and a portion of the inner leads to maintain stability of the structure. Instead, Minamio

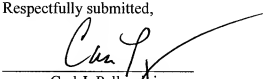
teaches a neck portion in the second lead (see Col. 8, lines 47-51; Col. 10, lines 18-33) and stepped portions formed around bonding pads (see Col. 10, lines 34-43) to maintain stability by providing a synergistic effect of stopping the progress of the stripping between the encapsulation resin and the leads (see Col. 10, lines 39-43).

In light of the above, one of skilled in the art, would not have been motivated to combine the teachings of Minamio with Yee to arrive at the method as defined by claim 25. Yee relates only to lead frame packages with single row of leads surrounding the die pad and therefore does not suggest any severing of post potions to create multi-rows of leads surrounding the die pad without affecting the stability of the IC structure and positions of the leads. If the skilled artisan were to refer to Minamio for guidance, with the aim of providing stability and maintaining positions of the leads in multi-row lead frame packages, he would be looking into developing neck portions or stepped portions which are taught by Minamio to maintain stability, and would clearly **not** have arrived at the combination of steps involving severing of post portions and die mounting on both the die pad and part of the inner leads, to provide stability to the overall IC package and maintain proper positions of the leads.

It is therefore respectfully submitted that claim 25 is not obvious in view of the combined teachings of Yee and Minamio. Claim 26, which is dependent on claim 25, is accordingly also not obvious.

The USPTO is directed and authorized to charge the statutory fee (37 C.F.R. §41.37(a) and 1.17(c)) and all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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Date: March 24, 2009

CLAIMS APPENDIX

Claims 25 and 26 are the claims on appeal.

25. A method of assembling an integrated circuit package, comprising:

a) providing:

a leadframe having a first face and a second face opposite to said first face, wherein said leadframe comprises:

an outer frame portion,

a die pad portion substantially centrally disposed within said outer frame portion,

a plurality of tie bars connecting said die pad portion to said outer frame portion, and

a plurality of protuberances extending substantially radially inward from said outer frame portion, each of said plurality of protuberances comprising an inner lead portion, an outer lead portion, and a post portion connecting said inner lead portion from said outer lead portion,

an integrated circuit chip having a first face and a second face opposite to said first face,

a first plurality of wires each having a first end and a second end, and

a second plurality of wires each having a first end and a second end;

b) disposing an adhesive layer on said first face of said leadframe, whereby said adhesive layer covers said die pad portion, and part of said inner lead portion of each of said plurality of protuberances, wherein part of each of said inner lead portions remains free of adhesive;

c) severing said outer lead portion from said inner lead portion by cutting said post portion;

d) mounting said integrated circuit chip on said leadframe, whereby said second face of said integrated circuit chip is connected to a first face of said die pad portion through said adhesive layer, and whereby said second face of said integrated circuit is further connected to said inner lead portions through said adhesive layer;

e) electrically conductively joining said first end of said first plurality of wires to a first face of one of said plurality of inner lead portions;

f) electrically conductively joining said second end of each of said first plurality of wires to said first face of said integrated circuit chip;

g) electrically conductively joining said first end of each of said second plurality of wires to a first face of one of said outer lead portions, and

h) electrically conductively joining said second end of said second plurality of wires to said first face of said integrated circuit chip.

26. The method according to claim 25, wherein the adhesive layer disposed on said first face of said lead frame in step (b) covers only an outer edge of said die pad portion, and part of said inner lead portion of each of said plurality of protuberances, thereby leaving a central part of said die pad portion and a part of each of said inner lead portions remains free of adhesive.

EVIDENCE APPENDIX:

This section is not applicable to the instant appeal.

RELATED PROCEEDINGS APPENDIX

This section is not applicable to the instant appeal.